



An Interview With Gary Smith

Gary Smith EDA, Inc.

(with the editors of the DAC.com Knowledge Center)

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DESIGN AUTOMATION CONFERENCE

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Editor's Note: Gary Smith is founder and Chief Analyst for Gary Smith EDA. Previously, he was the Managing Vice President and Chief Analyst of the Electronic Design Automation Service, Design & Engineering Cluster at Gartner Dataquest. He is editorial chair of the IEEE Design Automation Technical Committee (DATC) and a past General Chair of the IEEE Electronic Design Processes workshop. In 2007, he received an ACM SIGDA Distinguished Service award. In this interview, Gary gives insights into his background as methodologist and analyst, as well as his thoughts on what the future holds for the EDA industry.

Q. Tell us a bit about yourself.

I'm from Stockton, California, from a family that dates back to the gold rush days. I went to college at the Naval Academy in Annapolis, Maryland. I've been playing bass in bands since I was 13 years old, and am a Blues Freak. After the Academy I got married and spent the next six years doing four cruises to Vietnam on old WWII Destroyers. We had two daughters, who have given me two granddaughters.

I got married to Lori Kate in 2004 and we now have Casey who is four and a half and who is quite a character. My interests outside of my family and music are history and oriental philosophy, especially Taoism.

Q. What led to your becoming an analyst for the EDA industry?

After I got out of the Navy I went into semiconductors, first into power semiconductors and then into RF semiconductors with TRW. One of the reasons I was hired at TRW was to bring some maturity to the group. I was 30 at the time.

I came up to the Valley in 1976 and consider myself a second-generation Valley engineer. That was with Signetics, just as we were moving from MSI to VLSI. I soon concentrated on the new 8-bit microprocessors that were just coming out. After that I took over responsibility for the custom designs that were starting to come in from the consumer and automotive industries.

One of my customers suggested I get into the CMOS gate array business, as he thought that that was the wave of the future. I therefore joined my first startup, Telmos, and then was hired to put together and run the Semicustom Division of the Americas for Plessey. From there it was my second startup, ES2 with (Sir) Robin Saxby, and then a turnaround job at IMI. By that time I was tired of being a suit and joined LSI Logic, working for Jen-Hsun Huang at the famous San Jose Design Center as his methodologist. I spent most of my time being an evangelist for RTL design.

As you can see, I enjoy being on the bleeding edge of technology. So when I retired I decided to become an analyst at Dataquest for EDA, the next bleeding-edge technology. The rest is history.

Q. So what are the key EDA challenges?

Parallel computing is our major challenge both for our software and for embedded software. Next is the cost of design. Both the silicon virtual prototype and the software virtual prototype are keys to lowering those costs. Just to be concrete, here's how I define these concepts. A *silicon virtual prototype* is a hardware virtualization platform that enables an RTL handoff of an SoC. A *software virtual prototype* consists of virtualization tools used to allow the embedded software programmer to develop software prior to completed silicon.

([Here is a link to definitions of all my key terms.](#)) There is a lot to do, and much of it lies beyond the realm of what we have considered traditional EDA. The concerns of the EDA community today reminds me of a quote from one of my favorite books, *The Hitchhiker's Guide to the Galaxy*: whatever you do, "Don't panic."

Q. If the key challenges are outside the scope of EDA today, then do EDA companies today – or the overall worldwide population of what, around 6,000 people in EDA R&D – have the right balance of skill sets and applications/design knowledge to meet the challenges?

Yes, we do! As far as parallel computing is concerned, we are on the bleeding edge of that technology, as we are the first of the non-niche applications that truly needs the speed that parallel computing provides.

Q. What are the top 3 biggest disruptions in EDA that people need to watch out for?

You need to broaden your vision to really see what's going on. Just as the march up the Moore's Law curve is at the heartbeat of EDA, the heartbeat of electronics is the EDA tool – silicon – computer cycle. Basically we improve our tools, so that designers can use the new computers to take advantage of the next silicon node, so that the computer industry can build faster computers (software – silicon – computer). Everything else – Consumer, Military, Automotive, Telecom, Industrial – is a spin-off of the cycle. I think when we went off the von Neumann architecture we lost track of that cycle. We were blinded by the lure of the consumer world and lost track of the foundation of electronics. The software portion now becomes far more important as it is now much closely connected to the computer architecture as realized in many-core silicon. So the three disruptions are many-core silicon, non-von Neumann computer architectures, and parallel software. Basically it's all connected.

Q. Where do you see centers of gravity shifting?

It obviously shifts to the software. Not only do we need to rewrite our software to take advantage of many-core computers, but we also need to deliver tools that help the embedded community develop parallel software for the firmware that runs the silicon. Of course, those tools probably will be adopted by the applications developers, which means there is a lot of money to be made.

Q. Really? You used to show an upside-down pyramid of market size, measured in terms of number of seats, as we went from system to architecture to RTL to physical to manufacturing handoff. And the price pyramid was right-side up with, e.g., free FPGA tools up near the top. By how much will the EDA sector be able to grow?

We are picking up two new markets. The first market is the new *system board designers*. These engineers use FPGAs but want tools that work at the ES Level. They prefer to use C/C++ for a language. That group is a little larger than the SoC designers we are targeting now, so that doubles our market. The second is the *embedded software designers*. These

are the guys that are faced with programming the many-core SoCs that we are now producing. That group is fifteen times larger than the SoC designers we are targeting now.

I also took a look at the open-source community at the end of last year. I had thought that half of the new embedded tools would be free. I found no one working on free parallel computing tools. My conclusion was that the complexity of these tools is too much of an R&D challenge for open-source.

Q. Where will new companies emerge in EDA?

As usual, where the problems are. The IC CAD area is always good as they need to meet new challenges at each silicon node. RTL is not a great area, especially as verification moves up to ESL. Of course ESL is hot, especially in the Embedded Software Automation (ESA) area.

Q. What boundaries between traditional business sectors or business models are blurring.

I think that the EDA Industry and ESA need to merge. Software is now our customers' biggest problem, and we should solve it for them. After all, EDA is on the bleeding edge of parallel computing, so we should use our knowledge to solve their problems.

Q. What do you make of messages such as "EDA 360" or the "collaborative ecosystem" keynote talks from foundries?

I think they are both trying to get us to look at the bigger picture. One of the main things that needs to happen is to get the cost of designing a new SoC down to \$25 million. That is almost all in EDA's lap right now, as we haven't produced a working Silicon Virtual Prototype. Now, we have done well, and made good progress on the Software Virtual Prototype, but we still have a ways to go. Once we achieve these objectives, the VCs will start funding semiconductor startups, and these startups will start buying tools and then silicon from the foundries – and everyone will be happy.

Q. So, according to the Design Cost Model that you supply to the ITRS roadmap, the SoC development is around \$50 million today, roughly half for hardware and half for software. Where are the opportunities for the 2X cost reduction, and which types of EDA revenue will necessarily shrink?

The software virtual prototype is already a \$90M market, and I expect the silicon virtual prototype to grow as fast once it is on the market. That places them both in the Killer App category. Killer Apps tend to become half a billion dollar markets.

Q. You see a lot of EDA startups. Is startup activity down or up, relative to historical levels? How have startups evolved their strategies (that lead to success) in recent years?

The main change is that they are bootstrapping their company through the initial phase of development. They are waiting as long as they can before getting VC funding. That gives them better control over their destiny and makes sure they walk away with some money once their exit strategy is executed. As far as the activity – it's down a little, but really not by that much. EDA is still a good place to start a company.

Q. In what specific areas are you seeing concentrations of startup activity – and what's your overall count of EDA startups today?

It's fairly widespread. However, the top category is analog, followed by synthesis, functional verification, and the combination of interoperability tools and enterprise tools. Last year we had 37 companies added to my WallChart. The average for that statistic over that past sixteen years has been 43.

Q. What do you recommend readers look out for on the DAC show floor?

Me, actually. I had pneumonia a few weeks ago and Lori Kate has insisted I rent a electric cart. It really is for health reasons; she'll kill me if she sees me walking the floor. And since I drive fast, and will have a lot of distractions, I'll probably run over a few people. On the other hand, my trusty orange blazer now has an important safety function! Other than that, there is always my [What to See @ DAC list](#) that you can download from my website www.garysmithEDA.com or pick up at my [7:30pm Sunday night presentation in Pacific Ballroom C at the Hilton](#). Here's a hint. Two areas hot this year that weren't even on my list a year ago are (1) functional verification and (2) the combination of interoperability tools and enterprise tools. Oh, and if you're coming to my [Monday morning pavilion talk](#), come early: [Bob Gardner \(EDAC\)](#), [Peggy Aycinena \(EDA Confidential and EDAMarket\)](#), [Mike Santarini \(Xilinx\)](#) and I have a surprise for you!

Thank you, Gary!