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Leveraging Diagnosis for Yield Analysis

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ARTICLE: Diagnosis and Yield

Leveraging Diagnosis for Yield Analysis

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Abstract—As technology nodes continue to shrink, reaching required IC yield levels is becoming increasingly difficult and time-consuming. Many yield problems are design-specific, and subtle defect mechanisms are more difficult to isolate.

EDA providers have developed new techniques to address some of the challenges with production yield. For example, Mentor Graphics offers diagnosis-driven yield analysis, which leverages production test patterns and scan failure diagnosis tools to identify yield limiters. When new solutions are proposed, many questions arise: Do these new techniques really solve yield problems? Will they replace existing tools and yield management solutions? And in a world where the fabless model rules, who really owns the yield problem?

This article describes how a diagnosis-driven yield analysis process supplements traditional yield management systems to dramatically reduce the time and cost to identify the root cause of yield loss. It also discusses the roles of fabless designers and foundries in the yield learning process.

I. BEYOND DFM AND DFY

Overcoming yield challenges is increasingly more difficult but critical to reaching time-to-market, product quality, and profitability goals for semiconductor companies. Yield management systems (YMS) are commonly used along with failure analysis (FA) to monitor the manufacturing and test process to identify when yield problems occur and determine the root cause. Once root cause has been identified, corrective action such as a process change, mask change, or containment can be taken. In this article, we will explore what role scan diagnosis plays in the overall yield analysis process and how a methodology called diagnosis-driven yield analysis can address yield challenges faces by the industry.

II. THE TRADITIONAL ROLE OF SCAN DIAGNOSIS

The process of determining root cause of yield loss typically involves three steps:

1. Separate devices exhibiting systematic issue(s) from those with random defects;
2. Identify similar fail modes across multiple failing devices; and
3. Localize and identify physical defects through physical failure analysis.

Scan diagnosis is an established software-based method developed for localizing defects on devices that fail manufacturing test. For years, scan diagnosis has been used to aid failure analysis in Step 3 of the yield analysis process shown above. A typical diagnosis solution determines the location and classification of a defect in a failing device based on the design description, test patterns used to detect the failure, and the failure data from the tester, as shown in Figure 1.

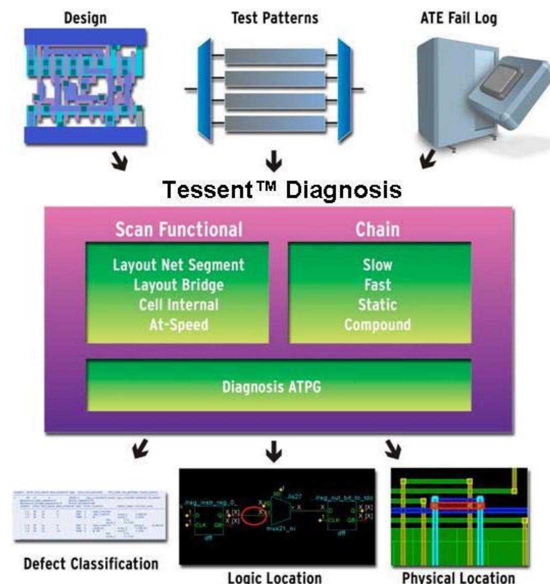

Figure 1: The inputs and outputs of the Mentor Graphics Tessent™ Diagnosis scan diagnosis tool.

Traditionally, scan diagnosis tools relied on the stuck-at fault model and could identify which logic net in the device that most likely contained a defect. This level of detail is not sufficient for effective yield analysis. For instance, multiple devices may have defects in different locations, but these defects may all be related to different instantiations of the same type of gate or be located in different net

segments containing the same type of via. Several recent advances in diagnosis technology have proven to increase the value of diagnosis in both yield and failure analysis:

- Layout-aware diagnosis leverages design layout to improve diagnosis resolution, eliminate physically impossible candidates, and provide reporting in terms of layout terms. Layout-aware diagnosis has proven to improve FA rates and turnaround time, reducing the search area by more than 90% [1].

- As much as 50% of defects can be internal to the cells. Cell-internal diagnosis ensures clear separation between defects in the interconnect ("back-end defects") and defects internal to the cells ("front-end defects"). This speeds up the PFA process and the overall yield loss factor analysis [2].

- 10% to 30% percent of logic failures are caused by scan chain defects [3]. Advanced chain diagnosis enables identification of scan chain defects and chain-functional compound defects [4].

- Delay defects typically represent 1% to 5% of the total defect population [5]. At-speed diagnosis provides clear identification of delay defects and timing errors [6].

III. SELECTION MATTERS

While physical failure analysis is ultimately used to confirm the root cause of yield loss, we first have to distinguish the devices that exhibit systematic issues from those with random defects. Assume that for a hypothetical product, there are on average 20 failing die per wafer. These failing die are typically evenly distributed across the wafer.

If, for one particular wafer, there is a total of 120 failing die, with a cluster of 100 in the center of the wafer, it is likely that *most* of the devices in this cluster represent the same underlying defect mechanism. *Some* of the defective die in the cluster may, of course, represent the normal distribution of random defects. In this particular case, if a handful of devices are selected for failure analysis, you can expect that the majority of these will represent the issue of interest.

In reality, however, separating random from systematic defects is more challenging. Assume that, in the previous example, one wafer has 40 failing die, and these appear to be evenly distributed across the wafer. If you randomly pick six die for failure analysis from this wafer, you can expect that three of these have defects related to the increased fall-out.
Instead, a selection process based on scan diagnosis results makes it possible to separate devices exhibiting systematic issue(s) from those with random defects and identify similar fail modes across multiple failing devices. Diagnosis-driven yield analysis uses statistical techniques to recognize correlations based on many different factors, helping to point you to views of the data that contain meaningful information [6].

For instance, while the distribution of failing die may appear to be random, the distribution of die with one particular diagnosis signature, such as devices failing for one particular type of standard cell, may be systematic in nature; as shown in the right wafer map in Figure 2.

This technique is called "zonal analysis," and is used in the Tessent™ YieldInsight™ tool from Mentor Graphics. This is one of many possible correlation techniques. With zonal analysis, the tool automatically examines the various diagnosis signatures of many failing die and flags those that have

an unexpected distribution across the dataset. A related approach is to correlate failures with DFM violations. No matter which cross-correlation technique is used, the intent is to separate the valuable results from the noise.

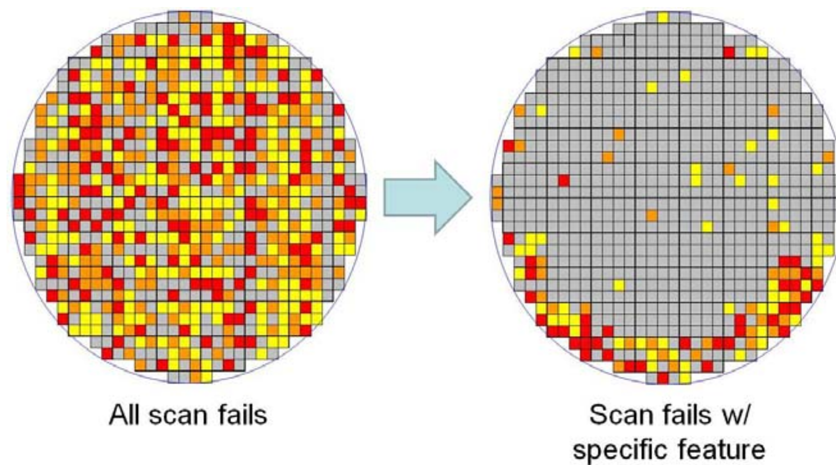

Figure 2: Separating systematic from random issues using volume diagnosis.

Once a specific feature, such as a specific standard cell type, is suspected of impacting yield, additional investigation into the data is performed to understand the impact of each systematic problem and to help select devices for physical failure analysis. By selecting devices that clearly exhibit the identified problem, and for which the diagnosis results are irrefutable, the failure analysis success rate is increased, and this reduces the time to verify the root cause.

Diagnosis-based yield analysis flows have been proven effective in several different cases. Appello et al. [7] demonstrated how such methods can identify design marginalities affecting circuit timing. Mekkoth et al. [8] showed that a systematic bridge defect caused by leftover metal residue could be identified by diagnosis and resolved by increased polishing. A new rule was also added to the bridge extraction deck, enabling further containment of this type of issues. Sharma et al. [9] identified the dominant defect mechanism causing a yield excursion to be an abnormality in a process step related to the fabrication of a specific type of via.

IV.DEPLOYING DIAGNOSIS-DRIVEN YIELD ANALYSIS

Diagnosis-driven yield analysis is most effective when data is collected and ready to be analyzed on a regular basis. In a diagnosis-driven yield analysis flow, scan diagnosis is integrated into the test and yield analysis process as shown in Figure 3.

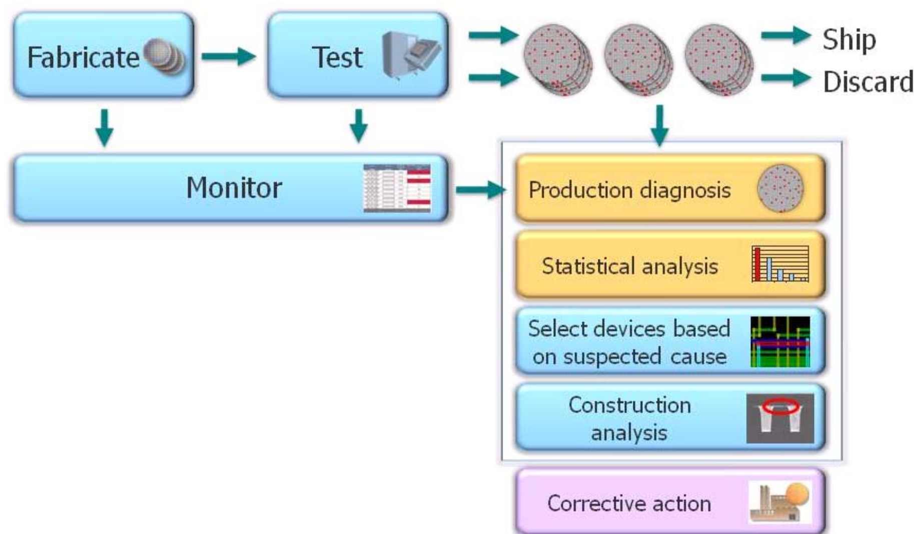

Figure 3: Diagnosis-driven yield analysis flow.

To implement a diagnosis-driven yield analysis flow, one must be able to manage the process of collecting failure data from multiple test systems and automatically performing volume scan diagnosis. A challenge is that different automatic test (ATE) platforms have different capabilities in terms of how much and how well they can collect data. In addition, there has been a lack of datalog format standards by which ATE operating systems can support failure data collection.

To be able to implement volume scan diagnosis, failures must be correctly logged with robust data traceability features—in a way that has no negative consequences for test quality and throughput. As production data collection is becoming more commonplace and the new STDF v4-2007 standard for data collection is adopted, these challenges are easier to overcome [10].

A yield-analysis flow based on scan diagnosis is not meant to replace all the other yield improvement techniques that are in use. Rather, it supplements established techniques. A yield management system continuously monitors data from multiple sources and provides a high-level view, quickly informing if something is going awry.

Diagnosis-driven yield analysis involves deeply diving into both the design and test failure data of the specific device, rather than relying only on manufacturing process data. Consequently, it can often provide more specific information to guide the physical failure analysis step, and can help uncover design-related systematic issues that are difficult to discover using process data alone.

While the issue of yield analysis has traditionally been associated more with IDMs and foundries, fabless semiconductor companies can also require the ability to analyze yield. A diagnosis-driven approach may be especially suitable in such a context, because the focus is on test results rather than manufacturing results.

Diagnosis-driven yield analysis can also be used to improve the effectiveness of DFM rules by correlating actual root causes to rules employed during verification, and setting higher priorities for

those rules that would mitigate the types of failures experienced. In this way, design sensitivities are uncovered to drive yield learning across many designs at a particular process node.

V. CASE STUDY

At STMicroelectronics, we dealt with a scenario that combined both new process technology and a new product introduction. The key objective in this investigation was to identify the root cause of lower than expected yield in a new (SoC) product that was manufactured using a new process technology.

With a new product in the early phases of new technology introduction, we expected to see several defect sources aliasing each other. In such a situation, the observed failures may appear to originate from a different defect mechanism than the one actually causing the failures. This was exactly what we were faced with.

In addition to having SoC yield and diagnosis information available, we also had corresponding information from a test chip (TC) for the same process.

Ideally, all process-related yield issues would be identified using TCs. TCs are specifically designed to explore yield performances of different layout configurations and to validate IP libraries. They typically consist of regular structures such as RAM and ROM or cell arrays. They also include ring oscillators and arrays of combinational and sequential logic cells. To make the result analysis as simple as possible, activation of the individual elements in a TC is made as simple as possible. This means, for instance, that test chips typically do not contain complex logic circuitry, since this would make it difficult to activate individual gates.

End product SoCs typically contain much more complex and irregular logic structures, defined by the functional design requirements. To activate and observe one particular cell in an SoC, one has to consider the circuitry connected to the input and output cones of this cell, as well as the additional circuitry affected by these logic cones.

In this particular scenario, the yield of the SoC was lower than the yield of the TC, despite the designs being comparable in size. Rather than being puzzled by this difference, we used it as a key data-point in the exploration, expecting that the cause of the low SoC yield could be related to the different architectural and topological complexity of the two designs.

In light of the gap between TC and SoC yields, the first analysis step that we took was to verify whether and how the yield was affected by any type of systematic marginality that was dependent on the SoC implementation. Examples of such dependencies could be timing-critical paths, crosstalk effects between adjacent wires, or power limitations. The verification for design-related systematic effects was done using volume scan diagnosis.

We expected that the failure signature would also include evidence of the problem. Simple cumulative analysis of the failure signature could indicate the presence of a systematic problem. Cumulative analysis of diagnosis results would enable location of the fault with better resolution.

However, no symptoms indicated design issues. We proceeded to filter out from the diagnosis results all signatures of a random nature. To identify random signatures, we used the fail data from the TC as well as comparative analysis across multiple sets of material.

The second analysis step that we took was to isolate any existing signatures. Here, the zonal analysis technique discussed above was of great help. We observed two combined factors:

1. A deterioration of performance moving from wafer border to center (see Figure 4).
2. Some core library cells showed a more prominent behavior of the same type.

Layout analysis of the identified cells causing these failures allowed us to recognize the layout features that these cells had in common, and identify criticalities associated with them.

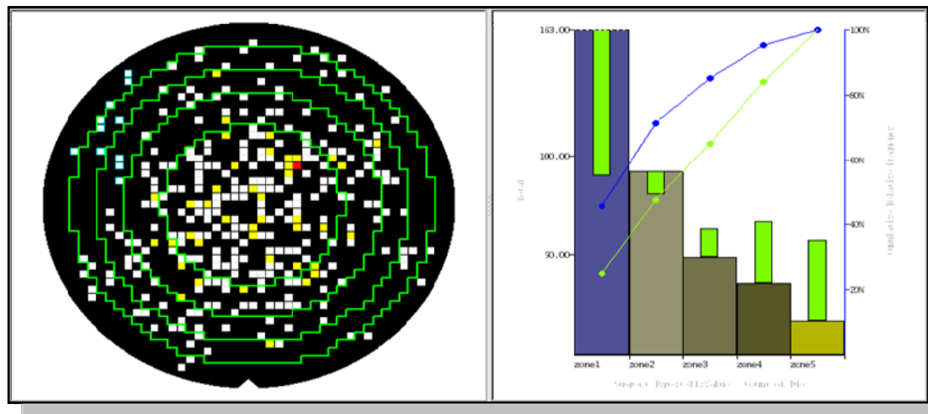

Figure 4: Center-border fail distribution effect.

As we believed we had identified a fail mechanism that caused the yield loss, the next step was to select a few die with the same signature. This selection was done based on the confidence of the diagnosis tool in the results. The subsequent physical analysis confirmed that the performance marginality was caused by improper centering of the process.

With a root cause identified, we were able to tune the manufacturing process. In parallel, we continued to observe the failure signature trend to verify that the critical signature was becoming negligible as a result of the process tuning and that no other systematic issues appeared.

VI. CONCLUSION

When properly used, the information hidden in test failure data can accelerate the yield analysis process. By setting up an infrastructure that captures and automatically diagnoses each manufacturing test failure, you can create a valuable database of information based on actual silicon results. When coupled with a diagnosis-driven yield analysis tool that performs statistical analysis on this large volume of diagnosis data, you can significantly reduce the time to recognize systematic yield issues and determine their root causes.

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