



Bringing MEMS Into the IC Design Flow

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Abstract— Micro-electromechanical systems have been available for years, and have been successful in selected high-volume applications. But MEMS design is not as widespread as it could be. MEMS design typically requires teams of expert specialists, and is mostly confined to IDMs that have their own fabs. Traditionally, there is little connection between the design of a MEMS device and the electronic circuitry it interacts with, and the handoff between MEMS and IC designers is ad hoc, manual and error-prone. This article describes the traditional MEMS design flow, discusses requirements for a “structured” and automated design flow, and shows an example flow that links a commercial MEMS 3D design environment with a custom IC design and simulation solution.

I. INTRODUCTION

Micro-electromechanical systems (MEMS) are micro-scale or nano-scale devices typically fabricated in a similar manner to integrated circuits (ICs) to exploit the miniaturization, integration, and batch processing benefits of semiconductor manufacturing. Unlike ICs, which consist solely of electrical components, MEMS devices combine technologies from multiple physical domains and may contain electrical, mechanical, optical or fluidic components.

MEMS may be invisible to the naked eye, but they've become ubiquitous in everyday life. Automobiles now contain numerous MEMS devices, including pressure sensors for engine control, accelerometers for crash sensing, and gyroscopes for stability control. Some consumer electronics products such as inkjet printers and digital light projectors (DLPs) have depended on MEMS for years, and recent years have seen an explosion in the integration of MEMS with electronics in mobile phones, cameras and gaming controllers.

Spurred by growth in consumer electronics, the total market for MEMS is projected to grow more than 40 percent from 2008 to 2012, from just over \$7 billion worldwide to over \$13 billion [1]. The market for MEMS in mobile phones is expected to grow by over 4X during this period to over \$2 billion.

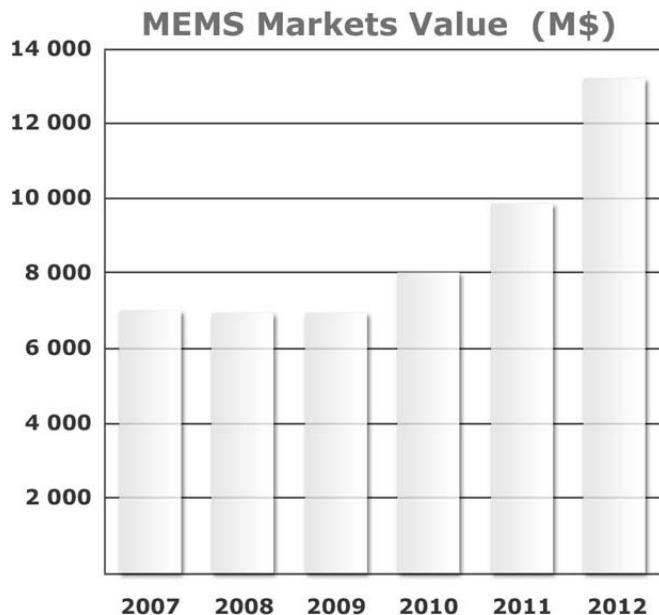


Figure 1: After several slow years, the MEMS market is expected to show rapid growth through 2012. Source: Yole Developpement [1].

As promising as these forecasts sound, only a few large IDMs are well-positioned to benefit from this rapidly growing market. This is due to the specialized expertise, long development time, and high costs of bringing MEMS devices to market. Although almost all MEMS devices are tightly integrated with electronics, either on a common silicon substrate or in the same package, MEMS design has traditionally been separated from IC design and verification.

MEMS devices are typically designed by PhD-level experts in such fields as mechanical, optical, and fluidic engineering. They use their own 2D and 3D mechanical CAD tools for design entry and

finite-element analysis (FEA) tools for simulation. Eventually the MEMS design must be handed off to an IC design team in order to go to fabrication, but the handoff typically follows an ad hoc approach that requires substantial design re-entry and expert handcrafting of behavioral models for functional verification.

Moreover, MEMS historically requires specialized process development for each design, resulting in a situation often described as “one process, one product.” While there are a number of specialized MEMS foundries, support from pure-play foundries has been very limited. Thus, most successful MEMS products on the market today were designed by teams of experts inside IDMs that have their own process technology. On average, according to one analyst report, it takes four years of development and \$45M in investment to bring a MEMS product to market [2].

Several trends are converging to make this level of effort and expertise unacceptable, not only for new entrants in the MEMS market, but for the best-positioned IDMs as well. First, the fast-paced consumer electronics market demands design cycles that are measured in months, not years. In addition to short time-to-market demands, consumer electronics companies must control design costs in order to maximize return on investment and profitability. \$45M investments in MEMS products are not sustainable in this market segment.

Second, the market is demanding more functionality from MEMS devices. For instance, STMicroelectronics recently announced a new product family that integrates 3-axis sensing of linear, angular and magnetic motion, plus pressure and temperature sensing, with necessary analog circuitry and a 32-bit microprocessor [3]. MEMS devices are also becoming more sensitive, and to enable this sensitivity, more analog and digital circuits will be placed around MEMS devices.

Third, advanced packaging technologies such as System-in-Package (SiP) and chip stacking (3D IC) with through-silicon vias will allow manufacturers to package all this functionality more densely, combining multiple MEMS sensors with analog and digital dice in a single package. These demands make MEMS systems more susceptible to unwanted coupling between sensing modes, and between the MEMS sensors and electronics.

The present approach to MEMS design, with separate design tools and ad hoc methods for transferring MEMS designs to IC design and verification tools, is simply not up to these new challenges. The time has come to “democratize” MEMS design and bring it into the IC design mainstream, so that design costs are reduced, time-to-market is shortened, and MEMS design is no longer confined to teams of specialists inside IDMs. One key to accomplishing this “democratization” is to build an integrated design flow for MEMS devices and the electronic circuits they interact with, using a structured design approach that avoids manual handoffs. This article discusses what such a flow might look like, and presents an example resulting from a recent collaboration between Coventor and Cadence Design Systems.

II. THE TRADITIONAL MEMS DESIGN FLOW

Before considering a structured MEMS-plus-IC design flow, let’s review the traditional MEMS design flow and its shortcomings.

While leading MEMS manufacturers have standardized their processes for certain types of MEMS, and use the same processes for derivative designs, it is still the case that a new MEMS design often requires process development. Thus, while the statement “one process, one product” is not always fully accurate, MEMS design tools must still be very much “process aware” in a way that is adaptable to arbitrary processes and process modifications.

In the absence of a cell library of basic building blocks, MEMS design traditionally starts with the physical design of the entire MEMS device in a 3D mechanical CAD environment or, occasionally, in a 2D layout tool. In the latter case, the layers are extruded or “booleaned” to form the desired 3D geometry. In either case, the geometry

may or may not be parametrized. The design is then simulated with time-consuming 3D finite element analysis, and changes are made until the simulated behavior meets the design goals.

Next, the MEMS design is handed off to IC designers. The IC designers work at several levels of abstraction, as illustrated in Figure 2. At the functional or algorithm level, MATLAB Simulink® from The Mathworks is often the tool of choice. The scope of the system that is simulated in Simulink may include software or firmware, digital logic, and analog circuits in addition to the MEMS itself. To support functional/algorithmic design in Simulink, the MEMS designers must manually create and hand off a model of the MEMS device in the MATLAB “M” language. Of course this MATLAB model must be kept in sync manually with any further changes in the MEMS design. But Simulink is not suitable for lower-level design and verification, nor does it provide a link to physical design.

At the architectural and implementation levels, the Cadence® Virtuoso® Layout Suite is commonly used for designing the analog/mixed-signal electronics that accompany a MEMS device. To support simulation of the electronics in the Cadence Virtuoso Multi-Mode Simulation environment, MEMS designers using a traditional flow manually create and hand off a model written in the Verilog-A hardware description language.

The handcrafted models developed for Simulink or the Virtuoso platform are most commonly based on analytic formulae, and less often on table lookups or model order reduction from finite element analysis. In the traditional flow, they don’t expose parameters of interest or allow IC designers to trade off accuracy for simulation speed. Nor do these models fully represent the behavior of the MEMS device. Typically, they are restricted to one mechanical degree of freedom, compared to six degrees of freedom in the actual device – 3 translations (x, y and z dimensions) and 3 rotations. Thus, for example, an accelerometer model would only model movement in one direction.

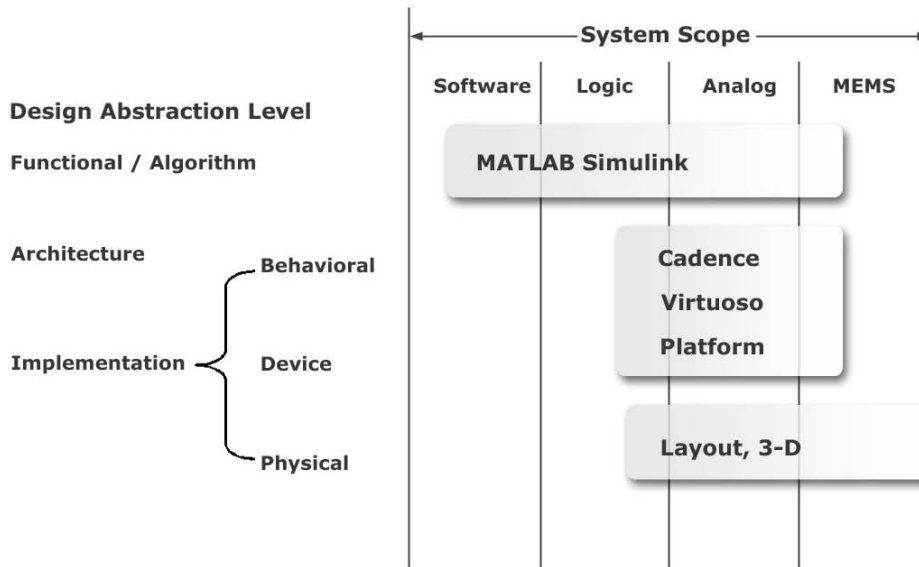


Figure 2: MEMS models must serve different EDA tools and abstraction levels.

To provide a path to manufacturing, the MEMS device must also be brought into a 2D IC layout system – e.g., the Virtuoso Layout Suite. Traditionally, MEMS designers manually redraw their layouts, because the MEMS layout used for manufacturing is not the same as the layout used for simulation. A visual inspection of the layout is often needed to make sure the MEMS device is properly connected to the electronic circuitry.

When the MATLAB and Verilog-A models are handcrafted and not parametric, any change to the MEMS design will force a rewrite or modifications of the model. Corner cases or manufacturing effects that might impact the performance of the MEMS device are typically not captured in the models. Therefore, any simulation that includes analog circuitry plus MEMS is likely to miss some effects. This

may cause an over-design of the analog circuitry, because designers are not exactly sure what they'll get from the MEMS device.

Moreover, handcrafting multiple MEMS models is time consuming, and requires specialized expertise. There is no assurance that the models at different levels are self-consistent, or consistent with the underlying physical design. Ideally, the MEMS designers could develop and maintain a "golden reference" for the MEMS design and automatically generate required simulation models for Simulink and Virtuoso Multi-Mode Simulation.

III. A STRUCTURED MEMS DESIGN FLOW

To bring MEMS design into the mainstream, the traditional ad hoc design flow needs to give way to a more automated, structured flow. The practice of rewriting models and redrawing layouts by hand is not compatible with the intense time-to-market pressures of consumer electronics. A structured flow would still have handoffs between MEMS and IC designers, but the handoffs would be much more automated. The modeling approach would be defined up front and be repeatable, rather than made up on the fly to suit each new design.

MEMS design needs to start with a well-characterized process. It is important to know the process parameters and material properties. Whether one is dealing with an external foundry or an in-house fab, MEMS designers need intimate process knowledge. Process variables, material properties, and geometric properties (lengths, widths, thicknesses) should be parametric to provide maximum flexibility for the MEMS designer.

A well-characterized library of reusable building blocks will greatly ease the MEMS development process. This library could include MEMS-specific electromechanical components such as beams, thin plates, plate electrodes, and electrostatic control drives that can be assembled into arbitrarily complex designs. Each building block should have a 3D view and an associated behavioral model.

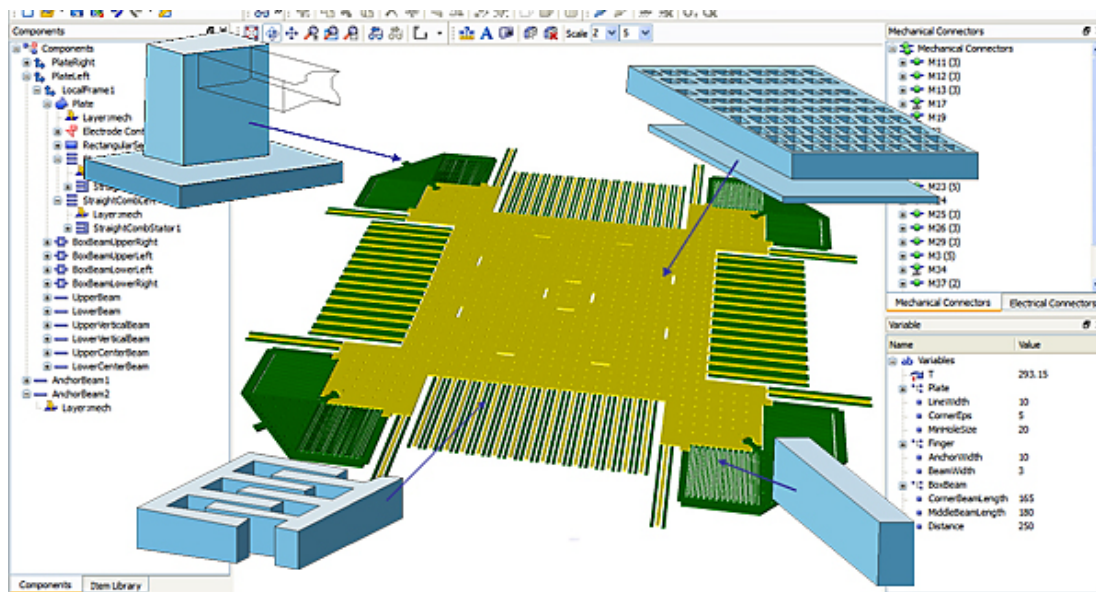


Figure 3: 3D design entry of a dual-axis accelerometer composed from MEMS building blocks (sketched in blue).

The MEMS designer will then assemble a device from these parameterized building blocks in a 3D environment. Ideally, there will be a single point of design entry. Once the design is entered, a

MEMS symbol can be brought into a system schematic. A parameterized layout cell, such as a SKILL language PCell, can be brought into a 2D physical layout that can then be converted into a GDSII file for fabrication. Engineers will not need to manually redraw layouts, and parameterization will allow changes to the MEMS device.

The MEMS device can also be simulated with its associated electronics in environments such as Simulink and Virtuoso Multi-Mode Simulation. Without careful attention to modeling, such multi-domain simulations can be very time-consuming. At the functional/algorithmic level, multi-domain simulations may encompass software and digital logic as well as analog circuits and MEMS. Accordingly, the MEMS behavioral model must sufficiently capture behavior, but require very little computational effort to make the multi-domain simulations possible in a reasonable amount of time.

At the behavioral level in Virtuoso Multi-Mode Simulation, it may be desirable to model the MEMS in more detail at the cost of somewhat longer simulation time. Ideally, the IC designer or MEMS designer will be able to trade off, as needed, the accuracy of the MEMS behavioral model for simulation speed.

The MEMS behavioral models must also support all types of simulations normally run for IC designs, including DC analysis, small-signal AC analysis, and transient simulations. Just as the accuracy-for-performance tradeoff is required for multi-domain simulations, it is also required to perform composite analyses such as Monte Carlo analysis, optimization studies, and process corners in reasonable time.

Extraction and design-rule checking will need to accommodate the MEMS device. If interconnects are part of the MEMS device, it will be necessary to extract the parasitics of that interconnect. The all-angle nature of MEMS devices may necessitate additional design rule checks. Also, checks may need to consider 3D criteria such as the vertical separation between components.

IV. EXAMPLE FLOW -- MEMS+ AND VIRTUOSO

The MEMS+™ product from Coventor, working in conjunction with the Virtuoso custom design platform from Cadence, provides an example of a structured MEMS-and-IC design flow that brings MEMS design into the EDA tool environment. MEMS+ is sold by Coventor as an adjunct to the Virtuoso platform, and will support Simulink as well in future releases.

To use MEMS+, MEMS designers enter designs in a natural 3D environment by selecting building blocks from Coventor's model library. This library can be thought of as the equivalent of the BSIM library in the IC design world – although it is proprietary rather than open-source. The library represents basic building blocks such as rigid and flexible plates, beam suspensions, and electrostatic comb drives.

Each building block not only has a 3D view, but also has an associated behavioral model. These models may be based on analytic formulae, numerical integration, or finite elements. Implementing these complex models in an HDL such as Verilog-A would be cumbersome and result in slow simulations, so Coventor has written them in C++ and provides them in binary form for portability and performance. The models take advantage of the native model interfaces available in Virtuoso Multi-Mode Simulation, including the Cadence Virtuoso Spectre Circuit Simulator, Cadence Virtuoso Accelerated Parallel Simulator, and Cadence Virtuoso UltraSim Full-Chip Simulator.

Upon importing a completed MEMS+ design, MEMS+ automatically generates a MEMS symbol that can be placed in the Virtuoso Layout Suite schematic. This is more than a “black box” showing only inputs and outputs – the MEMS designer can choose to expose parameters that may be of interest to the IC designer. In addition, MEMS+ automatically generates a netlist that contains references to the MEMS behavioral models. This makes it possible for an IC designer working in the Virtuoso platform to simulate the mechanical MEMS device along with the analog circuitry around it without having any special MEMS or mechanical CAD knowledge.

The simulation results can be brought back into the Coventor MEMS+ environment so MEMS designers can visualize the results in 3D. Further, because the MEMS designer still needs to verify the device on the physical implementation level, MEMS+ automatically generates 3D solid models that can serve as input to finite element analysis. Finally, MEMS+ can also automatically generate a fully parameterized SKILL PCell that has the same exposed parameters as the schematic symbol (Figure 4).

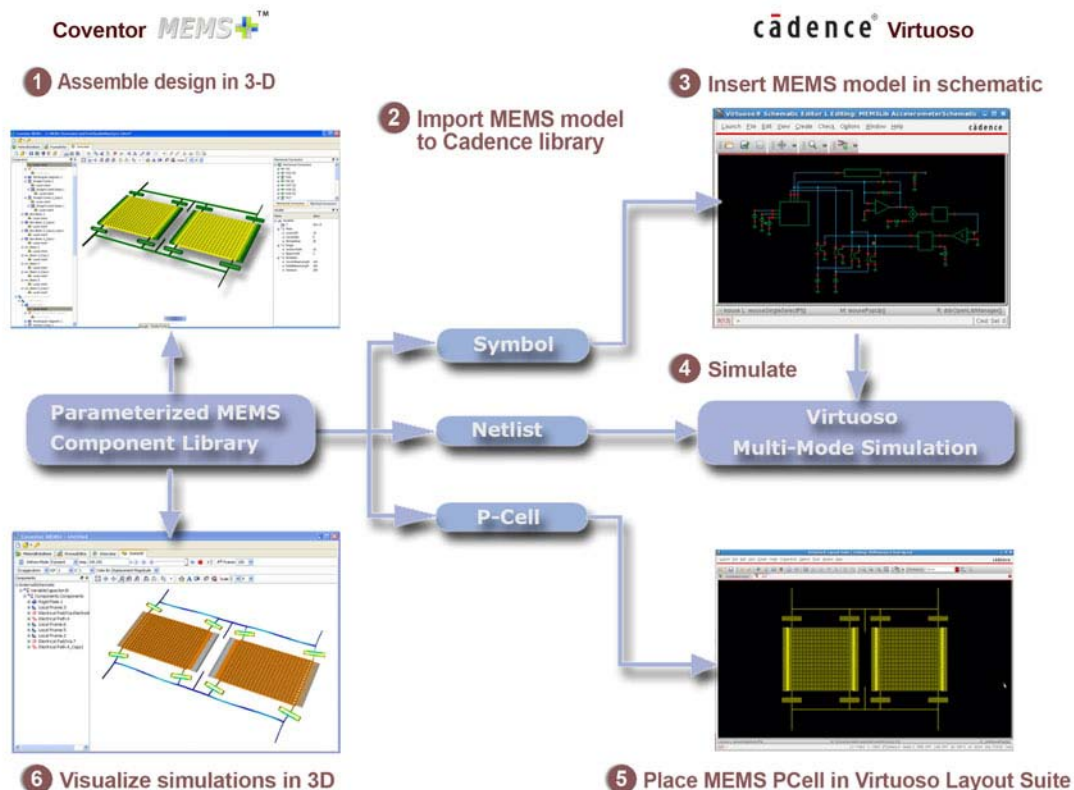


Figure 4: MEMS+ works closely with the Cadence Virtuoso custom design platform, linking MEMS design to schematics, simulation, and layout.

Thus, as shown in Figure 4, a design entered in MEMS+ can serve as the “golden source” for all levels of design abstraction, including simulation and implementation in the Virtuoso platform. It is worth noting that all aspects of the design are parameterized in MEMS+. This includes geometric properties, material properties, and process parameters. The MEMS designer can choose which parameters to expose to system and IC designers, and which to keep hidden.

V. FOUNDRY SUPPORT

With tooling now available to provide a structured design flow that links MEMS design with the IC design environment, the next priority is support from pure-play foundries. A foundry ecosystem with reference flows, silicon IP libraries, and process design kits is needed. When such an ecosystem is available, electronic systems developers can finally break free from the “one process, one product” tradition, and MEMS design will become more accessible to fabless companies. MEMS designs will also offer the potential to generate income for the foundries by driving business to the mature process nodes that MEMS designs are likely to use.

VI. CONCLUSION

MEMS devices offer great potential for continuing the pace of miniaturization that began with Moore's Law. They have already enabled great advances, from safer cars to digital projection, and are increasingly revolutionizing the way we interface with the latest multi-function consumer electronics. But MEMS design has for too long been confined to specialists who use an ad-hoc design methodology with little or no connection to the electronic design environment.

In this article, we have seen how traditional MEMS design flows involve manual hand-offs to IC designers, making it necessary to rewrite models and redraw layouts. A more structured, automated flow can overcome these deficiencies. The Coventor MEMS+ environment, working with the Cadence Virtuoso custom design platform, provides an example of a structured flow that helps automate the connection between MEMS design and IC design.

REFERENCES

- [1] J.C. Eloy, *Overview of MEMS Markets from Equipment to Devices: Where are the Remaining Areas of Growth Potential?* Semicon West 2009, San Francisco, CA .
http://www.semiconwest.org/cms/groups/public/documents/web_content/ctr_030869.pdf
- [2] Yole Developpement presentation, *Status of the MEMS Industry: What are the Current Growth Areas?* Semicon Japan, 2009.
- [3] STMicroelectronics press release <http://pddnet.com/news-stmicroelectronics-boosts-realism-and-accuracy-in-various-applications-021110/> .